REMARKS

Reconsideration of this application, as amended, is respectfully requested.

As a preliminary matter, in the Final Office Action mailed 02/17/2005, the Examiner did not attach an initialed copy of the PTO-1449 form listing references that were mailed to the PTO with an Information Disclosure Statement submitted on 10/04/2004. The Examiner also did not indicate the references on said PTO-1449 form were not in conformance with MPEP 609. As such, applicant respectfully requests that the Examiner indicate that these references have been considered and made of record.

Office Action Rejections Summary

Claims 1-3, 11 – 13 and 16 – 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,970,067 of Sathe et al. (hereinafter "Sathe") in view of U.S. Patent No. 5,764,637 of Nishihara (hereinafter "Nishihara"). Claims 4, 5, 14, 15, 19 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,970,067 of Sathe et al. ("Sathe") in view of U.S. Patent No. 5,764,637 of Nishihara ("Nishihara") in further view of U.S. Patent No. 6,449,658 of Lafe et al. ("Lafe").

Status of Claims

Claims 1 – 5 and 11 – 20 remain pending in this application. Claims 1, 11, and 16 have been amended. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter. No new claims have been canceled. Applicant reserves all rights with respect to the Doctrine of Equivalents.

Rejections Under 35 U.S.C. § 103(a)

Claims 1 – 3, 11 – 13 and 16 – 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sathe in view of Nishihara. Applicant respectfully submits that claims 1 – 3, 11 – 13 and 16 – 18 are patentable over Sathe in view of Nishihara. Independent claims 1,

11, and 16 each include the limitation of "writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer, wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer." Sathe discloses an ATM communication system in which a series of communication cells are multiplexed over a set of communication links. In particular, Sathe includes the following disclosure:

> The state machine 84 sequences the inbound communication cells from the framing and line interface circuits 80-82 into the inbound delay compensation buffer 96. The state machine 84 filters out idle communication cells received over the communication links 1-N. The state machine 84 extracts the inbound master framing sequence on each communication link 1-N and stores the inbound communication cells into inbound delay compensation buffer 96 according to the corresponding master framing sequence. Inbound communication cells are sequenced out of the inbound delay compensation buffer 96 and stored in the inbound cell buffer 86 in the original cell sequence using a cell read pointer. The cell read pointer follows the link write pointers 1-N around the link buffers 1-N in a circular fashion. ***The cell read pointer follows the link write pointer 1-N that corresponds to the communication link 1-N having the longest delay in communication cell transmission between the communication nodes 26 and 28***. The master framing sequence on each communication link 1-N provides an indication of the relative phase delay for each of the communication links 1-N. The cell read pointer is only updated after an inbound communication cell corresponding to the communication link 1-N having the longest delay is stored into the inbound delay compensation buffer 96 in the appropriate link buffer 1-N.
>
> (emphasis added) (Sathe, col. 10, lines 21 – 44, and Fig. 10)

As such, nothing in Sathe discloses or suggests that the write pointer for the inbound delay compensation buffer varies from another write pointer corresponding to another data link and a delay compensation buffer.

Nishihara discloses an STM/ATM converter for converting time-slot data in STM frames to ATM cells. In particular, Nishihara includes the following disclosure:

> That is, STM data is written into a cell block by each byte data basis. The writing address table 207 contains a cell block address which is now being written for each virtual path and the offset address in the cell block. When writing STM data into a cell block for a certain virtual path starts for cell assembly, the writing address table 207 is referred with the virtual path identifier number and the writing address 211 (cell block address

> corresponding to the virtual path) and the offset address in the cell block 210 are given to RAM (the cell buffer) 201. At this time, the queue length control section 206 instructs the writing address table 207 to increment the value by one for updating offset address value in the table 207. The queue length control section 206 writes the cell block address to the FIFO 205 corresponding to the virtual path when the offset address value having been incremented reached to the predetermined value, for example, 48 bytes (equals to the size of ATM cell payload segment).
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> (Nishihara, col. 5, lines 40 – 56, and Figure 3)

Nothing in Nishihara discloses or suggests that STM data is written into a delay compensation buffer, let alone the use of different write pointers. As such, Nishihara fails to cure the deficiency of Sathe.

Examiner states that, "[I]t would have been obvious to one ordinary skilled in the art to use the cell reading method of Nishihara into the node 28 of Sathe et al. in order to read cells from delay buffet faster than cells written into the buffer" (02/17/05 Final Office Action, page 3, lines 13 – 17). Applicant respectfully submits that Sathe does not disclose or suggest a combination with Nishihara and that Nishihara does not disclose or suggest a combination with Sathe. It would be impermissible hindsight based on applicant's own disclosure to incorporate the STM/ATM converter of Nishihara into the ATM communication system of Sathe.

Even if Sathe and Nishihara were somehow combined, such a combination would still lack the limitation of "writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer, wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer." Therefore, applicant respectfully submits that independent claims 1, 11, and 16 are patentable over Sathe and Nishihara under 35 U.S.C. § 103(a) and request removal of the rejection.

Claims 2 – 3 depend directly from claim 1, claims 12 – 13 depend directly from claim 11, and claims 17 – 18 depend directly from claim 16. As such, claims 2 – 3, 12 – 13, and 17 – 18 also include the limitation of "writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer,

wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer." Therefore, applicant respectfully submits that independent claims 2 – 3, 12 – 13, and 17 – 18 are also patentable over Sathe and Nishihara under 35 U.S.C. § 103(a) and request removal of the rejection.

Claims 4, 5, 14, 15, 19 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Sathe in view of Nishihara, and further view of Lafe. Applicant respectfully submits that claims 4, 5, 14, 15, 19 and 20 are patentable over Sathe, Nishihara, and Lafe. Claims 4 – 5 depend from independent claim 1, claims 14 – 15 depend from independent claim 11, and claims 19 – 20 depend from independent claim 16. As such, claims 4 – 5, 14 – 15, and 19 – 20 each include the limitation of "writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer, wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer." As discussed above, nothing in Sathe or Nishihara discloses this limitation.

Lafe discloses a method for accelerating data transport through communication networks. In particular, Lafe includes the following disclosure:

> In accordance with a preferred embodiment of the present invention, data acceleration is achieved by replacing the Client's slow connection with a compressed link to the Accelerator Server, as will be described below. This allows the user to transfer large amounts of data more quickly over the slow connection. The Accelerator Server is connected to the Internet or a corporate intranet by a high-speed connection. The effect is that the user realizes much higher data transfer speeds, because the same amount of data can be transferred in less time.
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> (Lafe, col. 5, lines 17 – 26)

Nothing in Lafe discloses or suggests the use of write pointers to write to different locations of delay compensation buffers. As such, Lafe fails to cure the deficiencies of Sathe and Nishihara.

It is also respectfully submitted that Sathe does not teach or suggest a combination with Nishihara and Lafe and that Nishihara does not teach or suggest a combination with Sathe and Lafe and that Lafe does not teach or suggests a combination with Sathe and Nishihara. It would be impermissible hindsight based on applicant's own disclosure to incorporate the STM/ATM converter of Nishihara and the data transport method of Lafe into the ATM communication system of Sathe. As such, applicant respectfully submits that claims 1, 11, and 16 are patentable over the combination of Sathe, Nishihara, and Lafe under 35 U.S.C. § 103(a) and request removal of the rejection.

Given that claims 4 – 5 depend from claim 1, claims 14 – 15 depend from claim 11, and claims 19 – 2- depend from claim 16, applicant submits that claims 4, 5, 14, 15, 19 and 20 are patentable over Sathe, Nishihara, and Lafe under 35 U.S.C. § 103(a) and request removal of the rejection.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,
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Date: 17 August 2005

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